

<p style="text-align: center;">9-18-07</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)</p>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Application Number</td> <td>10522262</td> </tr> <tr> <td>Filing Date</td> <td>2003-07-18</td> </tr> <tr> <td>First Named Inventor</td> <td>Jiro Hietanen</td> </tr> <tr> <td>Art Unit</td> <td>2811 2815</td> </tr> <tr> <td>Examiner Name</td> <td>To Be Assigned shingleton</td> </tr> <tr> <td>Attorney Docket Number</td> <td>800186US</td> </tr> </table>	Application Number	10522262	Filing Date	2003-07-18	First Named Inventor	Jiro Hietanen	Art Unit	2811 2815	Examiner Name	To Be Assigned shingleton	Attorney Docket Number	800186US
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U.S. PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/MBS/	1	4227942		1980-10-14	Hall	
/MBS/	2	4626613		1986-12-02	Wenham et al.	
/MBS/	3	4984358		1991-01-15	Nelson	
/MBS/	4	5468852		1995-11-21	Gee	
/MBS/	5	6836020		2004-12-28	Cheng et al.	
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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/MBS/	1	E.M. CHOW ET AL., "Electrical Through-Wafer Interconnects and Microfabricated Cantilever Arrays Using Through-Wafer Silicon Etching," Thesis at Stanford University, August 2001, 196 pages.	<input type="checkbox"/>
/MBS/	2	E.M. CHOW ET AL., "Process Compatible Polysilicon-Based Electrical Through-Wafer Interconnects in Silicon Substrates," Journal of Microelectromechanical Systems, December 2002, pp. 831-840, Vol. 11, No. 6, IEEE.	<input type="checkbox"/>
/MBS/	3	C.H. CHENG ET AL., "An Efficient Electrical Addressing Method Using Through-Wafer Vias for Two-Dimensional Ultrasonic Arrays," IEEE Ultrasonics Symposium, 2000, pp. 1179-1182.	<input type="checkbox"/>
/MBS/	4	C.H. CHENG ET AL., "Electrical Through-Wafer Interconnects with Sub-PicoFarad Parasitic Capacitance," IEEE Microelectromechanical Systems Conference, 2002, pp. 18-21.	<input type="checkbox"/>
/MBS/	5	V. CHANDRASEKARAN ET AL., "Through-Wafer Electrical Interconnects for MEMS Sensors," Proceedings of ASME International Mechanical Engineering Congress and Exposition, November 2001, pp. 1-6.	<input type="checkbox"/>

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EXAMINER SIGNATURE

Examiner Signature	/Michael B Shingleton/	Date Considered	4-15-2009
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

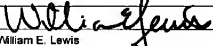
☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	2008-12-04
Name/Print	William E. Lewis	Registration Number	39,274

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.